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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/749,734	12/30/2003	Yibin Ye	110350-134110	9041

31817 7590 05/04/2005

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EXAMINER	
LE, THONG QUOC	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 05/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·B

Office Action Summary	Application No.	Applicant(s)	
	10/749,734	YE, YIBIN	
	Examiner	Art Unit	
	Thong Q. Le	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 3/18/05.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17 and 21-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17 and 21-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Amendment filed on 03/18/2005 has been entered.

2. Claims 1-17,21-23 are presented for examination.

Response to Arguments

3. Applicant's arguments with respect to claims 1-23 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-17,21-23 are rejected under 35 U.S.C. 102(b) as being anticiapted by Van der Wagt (U.S. Patent No. 5,953,249).

Regarding claim 1, Van der Wagt discloses a two-transistor DRAM cell (Fires 2a-2c) comprising:

a NMOS device with a first gate (Figure 2a-2d) ; and

a PMOS device with a second gate (Figures 2a-2d), the PMOS device -coupled to the NMOS device; and

a storage node (SN) coupled to at least one of the first and the second gates.

Regarding claim 2, Van der Wagt discloses wherein a the storage node is defined between the PMOS device and the NMOS device (Figure 2 SN), the storage

node having a voltage that converges to Vhigh, where Vhigh is greater than Vcc/2 (Figure 5), and further comprising: an n-channel (NMOS) device (Figure 3, 22) coupled between the read bit line (Figures 3-4, BL) and the read word line (READ WL); and a p-channel (PMOS) device (Figure 3, 20) coupled to the NMOS device so as to define a storage node therebetween.

Regarding claims 4, 11, 21 , Van der Wagt discloses a DRAM cell (Figure 4) comprising:

a read bit line (BL);

a write bit line (BL) ;

a read word line (READ WL);

a write word line (WRITE WL);

an n-channel (NMOS) device (22) coupled between the read bit line and the read word line; and

a p-channel (PMOS) device (20) coupled to the NMOS device so as to define a storage node (SN) therebetween.

Regarding claims 5-10, 12-17,22-23, Van der Wagt discloses the PMOS device (Figure 3, 20) is coupled between the write bit line and a gate region of the NMOS device (Figures 2a-2d, 3-4), and PMOS device comprises a gate region coupled to the write word line (Figure 3, gate of 20 coupled to WRITE WL), and wherein the write word line is pulled from a logic high voltage to a logic low voltage to write data into the DRAM cell (Figure 4), and wherein the read word line, the read bit line and the write word line are held at a logic high voltage to hold data within the DRAM cell (Figure 4), and

wherein the data written into the DRAM cell corresponds to the voltage level of the write bit line (Figure 4), and wherein a voltage level of the storage node converges to logic high due to edge leakage current (Figures 2), and wherein the IC comprises a central processing unit, and at least one input/output module coupled to the central processor unit, and wherein the memory is coupled to the IC via the communication channel (Column 1, lines 10-27).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai V. Ho can be reached on 571-272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thong Q. Le
Primary Examiner
Art Unit 2827

THONG LE
PRIMARY EXAMINER